AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 9, which starts with "This application is related", with the following amended paragraph:

This application ~~is related to provisional patent application Serial~~ claims the benefit of U.S. Provisional Application No. 60/142,132, filed on July 2, 1999, the contents of which are incorporated herein by reference. This application is related to U.S. Patent Application Serial No. 09/421,279, entitled "SMART CARD SYSTEM AND METHODS FOR PROVING DATES IN DIGITAL DATA FILES," filed October 20, 1999; U.S. Patent Application Serial No. 09/609,646, entitled "SYSTEM AND METHODS FOR PROVING DATES IN DIGITAL DATA FILES," filed July 3, 2000; and U.S. Patent Application Serial No. 09/609,645, entitled "SYSTEM AND METHODS FOR PROVING DATES IN DIGITAL IMAGING FILES," filed July 3, 2000.

Please replace the paragraph beginning on page 20, line 6, which starts with "Referring now to Fig. 7", with the following amended paragraph:

Referring now to Fig. 7, a block diagram of a presently preferred embodiment of the PC system 700 according to the present invention is shown. System 700 generally comprises a server 720, having a keyboard 740 and mouse 760 attached thereto for inputting digital data into the server 720, ~~fraud prevention means 760~~ fraud prevention means 560 for proving with certainty the dates and times that digital data files contained within the server 720 were accessed, created, modified, stored, or transmitted, and a monitor 780 for displaying such files. As an option, server 720 may include ~~verification means 780~~ verification means 580, which are adapted to verify the authenticity of a date and time-stamp affixed to such digital data files.

Please replace the paragraph beginning on page 20, line 13, which starts with "According to one presently preferred embodiment", with the following amended paragraph:

According to one presently preferred embodiment of this invention, the ~~fraud prevention means 760~~ fraud prevention means 560 is contained within the server 720 in the form of its motherboard 800 (Fig. 8). One such motherboard 800 is manufactured by Intel Corporation, Santa Clara, California U.S.A., under the model name "N440BX Server". ~~It is a~~ Motherboard 800 is a flat "baseboard" design and features a dual Pentium® II processor-based server system that provided a high-performance platform optimized for 100 MHz system bus operation. Thus, motherboard 800 is equivalently embodied as baseboard 800, as described in detail below.

Please replace the paragraph beginning on page 22, line 10, which starts with "An embedded SVGA-compatible", with the following amended paragraph:

An embedded SVGA-compatible video controller 814 is also provided on baseboard 800. It preferably comprises a CL-GD5480 64-bit SGRAM GUI Accelerator, manufactured by Cirrus Logic, Inc., Fremont, California, U.S.A. Further details regarding such accelerators may be found in the "CL-GD5480 Advance Data Book, Ver. 1.0 (November 1996), which is incorporated herein by reference. The SVGA subsystem also contains 2MB of SGRAM (*i.e.*, synchronous ~~graphics RAM) 816~~ graphics RAM) 815, which is typically provided as a factory build option and is not upgradeable.

Please replace the paragraph beginning on page 24, line 33, which starts with "The PIIX4 820 contains", with the following amended paragraph:

The ~~PIIX4 820~~ baseboard 800 contains a real-time clock 830 with battery backup from an external battery 832. It also contains 242 bytes of general purpose battery backed CMOS system configuration RAM. On the baseboard 800, these functions are duplicated in the SuperI/O ~~chip 814~~

chip 834. However, in accordance with yet another important aspect of the present invention, real-time clock 830 shown in Fig. 8 is replaced with a more secure, tamperproof version as follows.

Please replace the paragraph beginning on page 26, line 20, which starts with "The "Multiplexed Bidirectional Address/Data Bus" comprises", with the following amended paragraph:

The "Multiplexed Bidirectional Address/Data Bus" comprises pins AD0-AD7, 1008, 1010, 1012, 1014, 1016, 1018, 1020, 1022, together which saves pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the real time clock 1000 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the real time clock 1000 latches the address from ~~AD0 to AD6 1008, 1010, 1012, 1014, 1016, 1018, 1020, 1022~~ AD0 to AD6, 1008, 1010, 1012, 1014, 1016, 1018, 1020. Valid write data must be present and held stable during the latter portion of the DS or WR pulses. In a read cycle the real time clock 1000 outputs 8 bits of data during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as RD transitions high in the case of Intel timing.